COLUMBIA | ENGINEERING
The Fu Foundation School of Engineering and Applied Science

ELEN E3106/4106 Lecture 22

MOSFETs Part II

Outline

- Energy band diagrams
- MOSFET as a barrier-controlled device
- Key device metrics and how to find them
- Basic quantitative current-voltage model

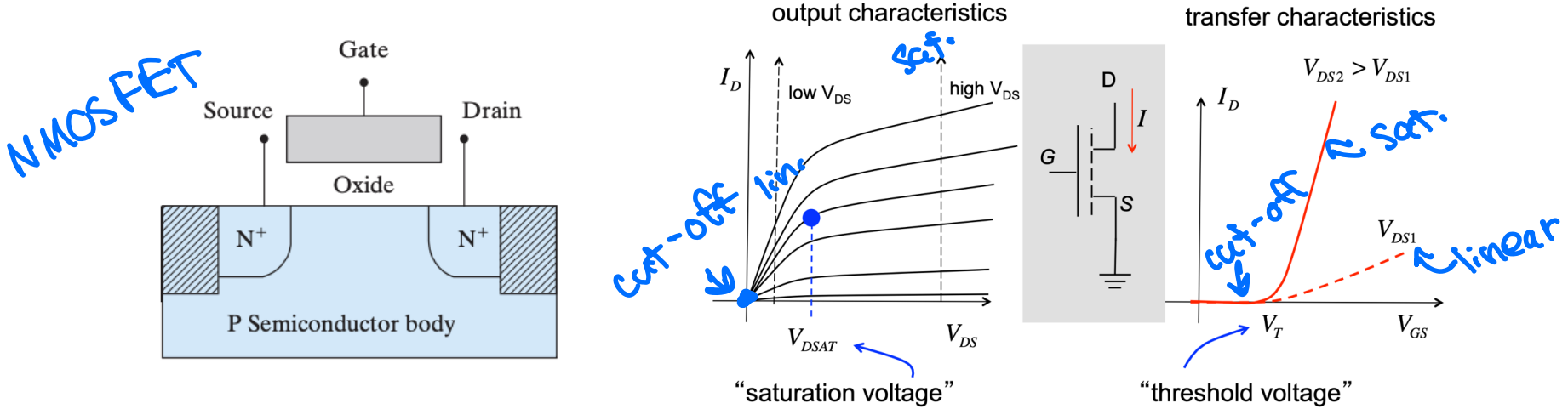
Assignments:

Homework 8 due Monday Dec. 1st by 11:59pm

Extra credit opportunity during in-class review session on Thursday December 4th

Recap so Far

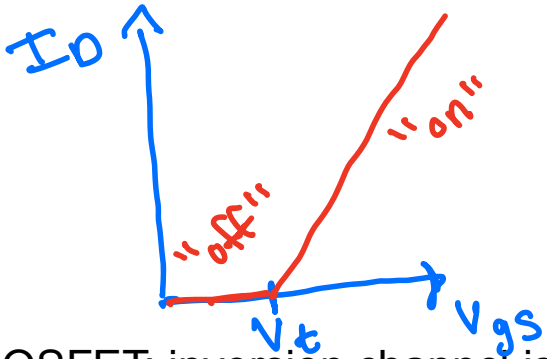
- MOSFETs are 3 terminal voltage-controlled (V_{gs}) current-sources (I_D)
- Field-effect: the gate voltage modulates the E-field and conductivity of the channel under the gate, effectively controlling the flow of current between source/drain
- Gate structure incorporates MOS cap. MOS cap inversion layer is called the conducting channel
- We discussed NMOSFETs , PMOSFETs, depletion-mode, enhancement-mode (normally off)
- Regions of operation: 1) cut-off 2 linear 3 saturation



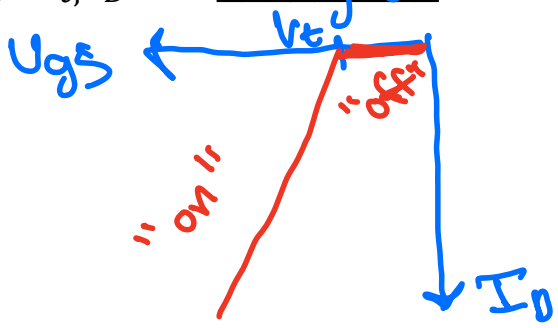
Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*, M. Lundstrom ECE 305 Slides

Recap so Far

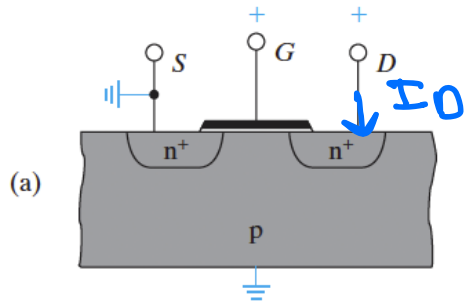
- NMOSFET: inversion channel is n-type, V_{ds}, V_{gs}, V_t, I_D are positive

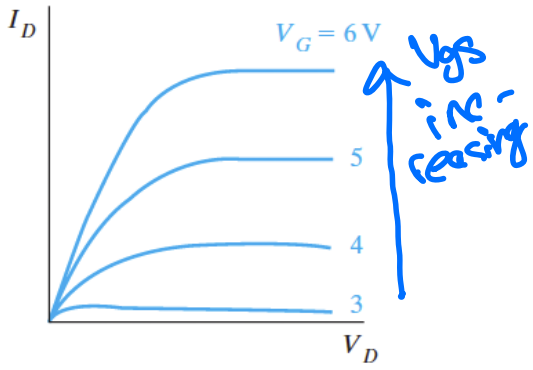


- PMOSFET: inversion channel is p-type, V_{ds}, V_{gs}, V_t, I_D are negative

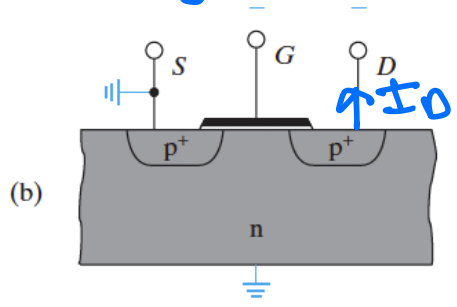


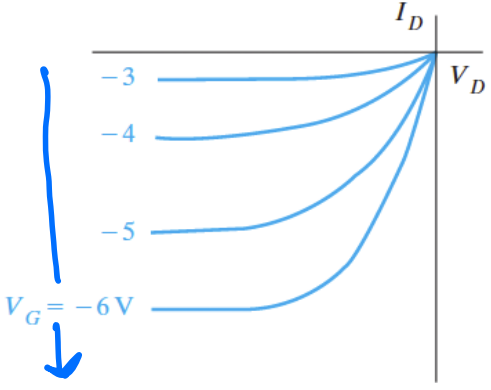
$V_g > V_t$ $V_D(+)$





$V_g < V_t$ $V_D(-)$





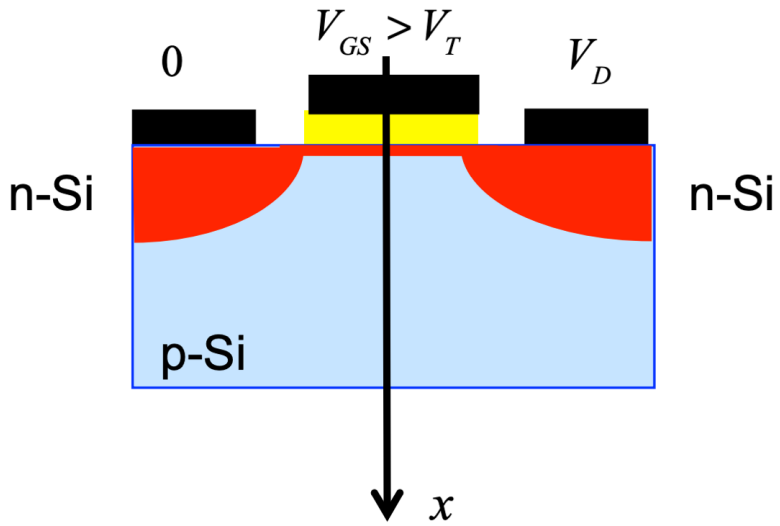
* Note the polarity

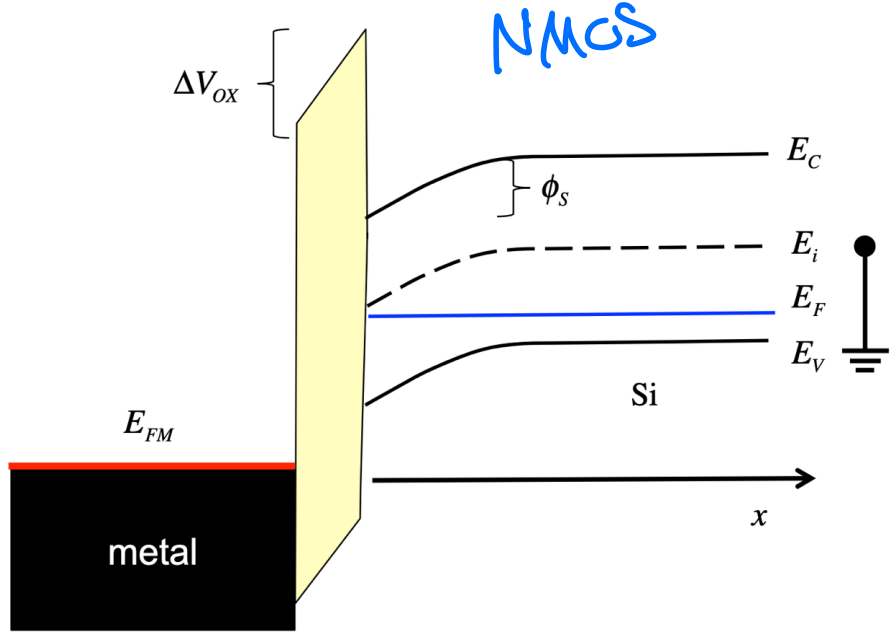
|Vgs| increasing

Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*

MOSFET Energy Band Diagram in Equilibrium

- Let's look at the MOSFET energy band diagram
- Normal to the channel, we have our MOS cap
- What type of MOSFET is this? N MOSFET

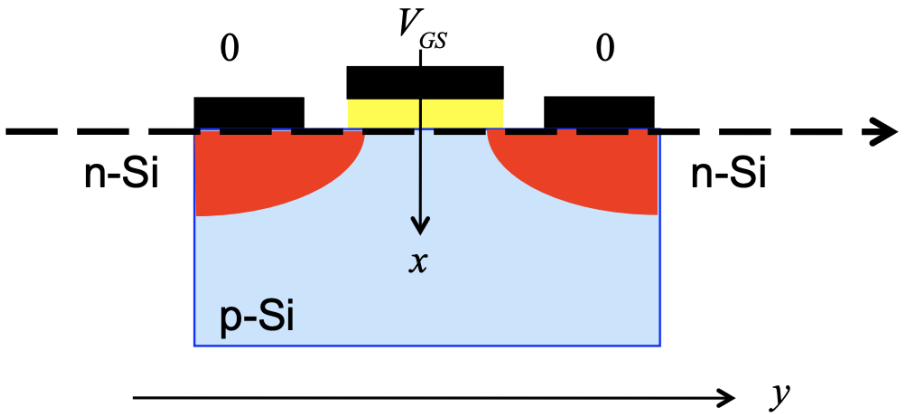


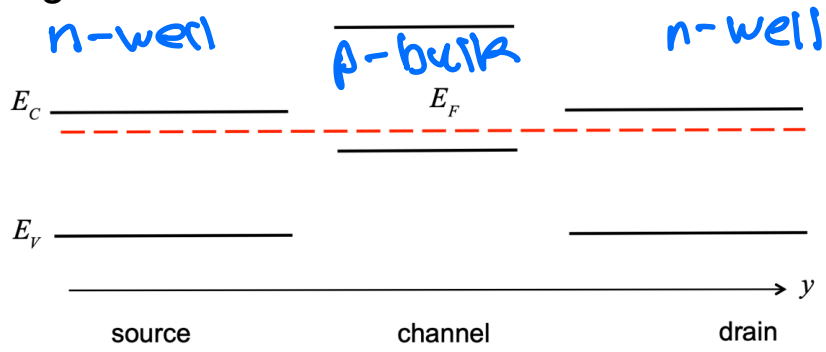


Sources: M. Lundstrom ECE 305 Slides

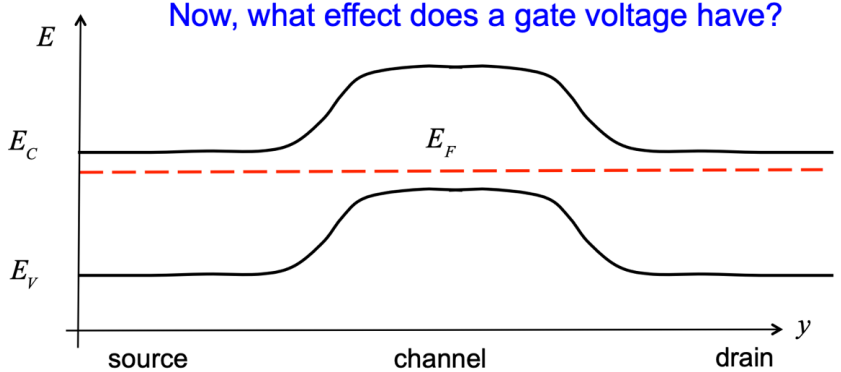
MOSFET Energy Band Diagram in Equilibrium

- Parallel to the channel, we have a similar structure to the npn BJT
- Recall: to draw our band diagrams in equilibrium, we first align the Fermi levels in the different regions, and then connect E_c and E_v





Now, what effect does a gate voltage have?

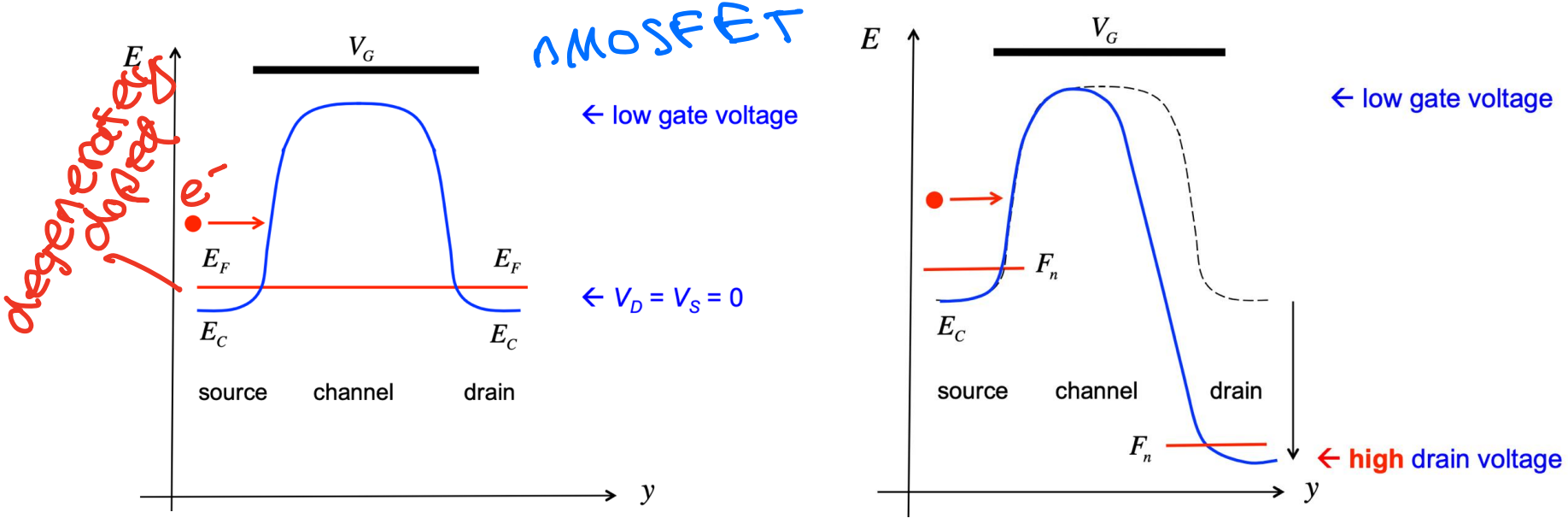


Sources: M. Lundstrom ECE 305 Slides

MOSFET As a Barrier-Controlled Device

- We can think of the channel under the gate as a barrier to e- flow
- The height of the barrier (and current flow) is modulated by the gate voltage
- Imagine we have a low $V_{gs} <$ Vt and $V_{ds} = 0$ (left)
- Even as we increase $V_{ds} > 0$, the barrier to e- from source to channel is still high (right)
- Device is still off -> very little I_D (cut-off mode)

nMOSFET

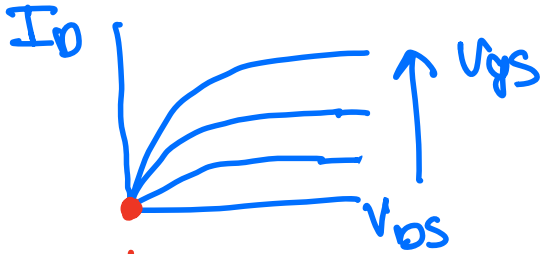


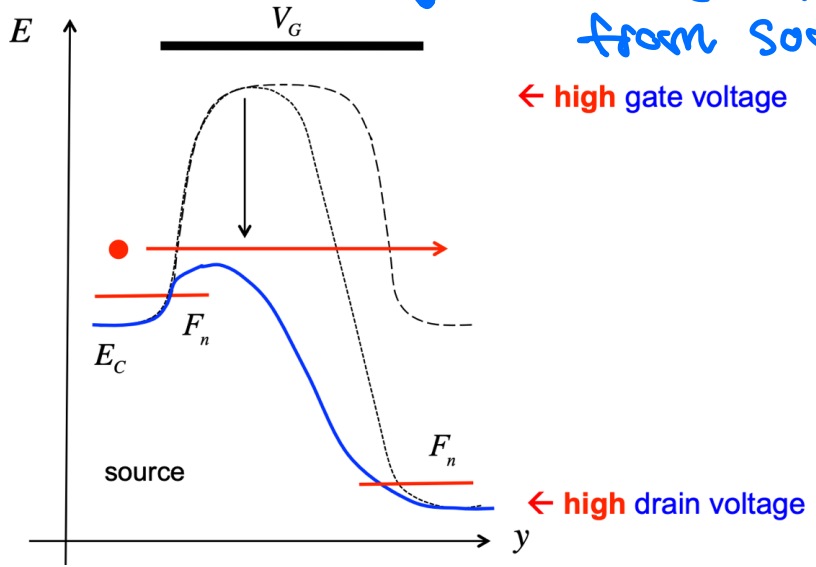
Sources: M. Lundstrom ECE 305 Slides

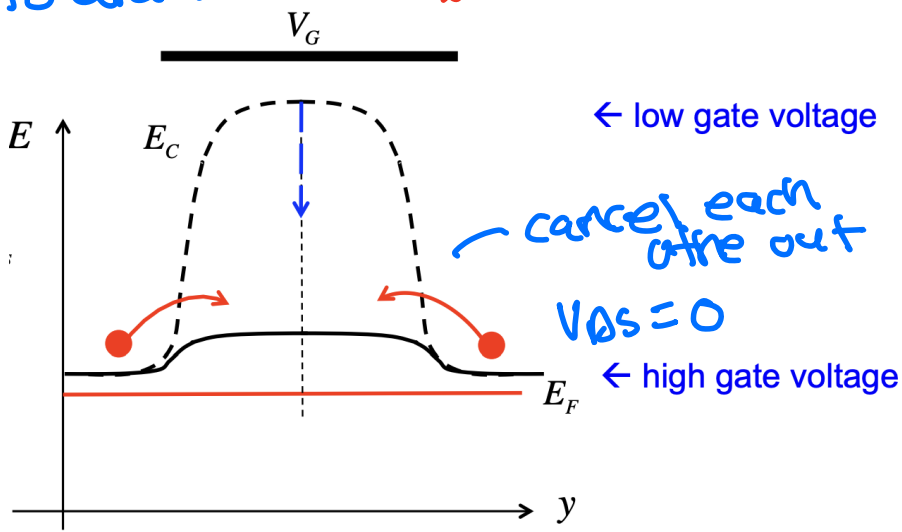
MOSFET As a Barrier-Controlled Device

- As we increase $V_{gs} >$ V_t we have lowered the barriers to e- flow
- A significant # of carriers are able to cross from source to drain
- The device is now "on" with significant I_D

We apply V_{DS} to ensure maj. of carriers move from source to drain



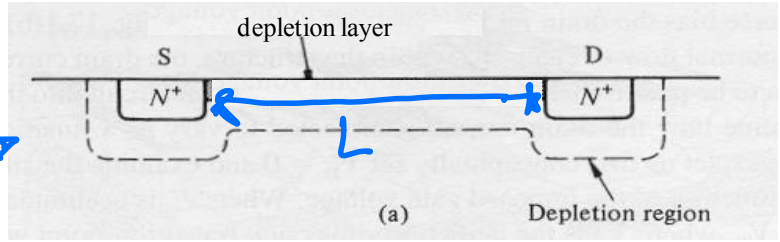




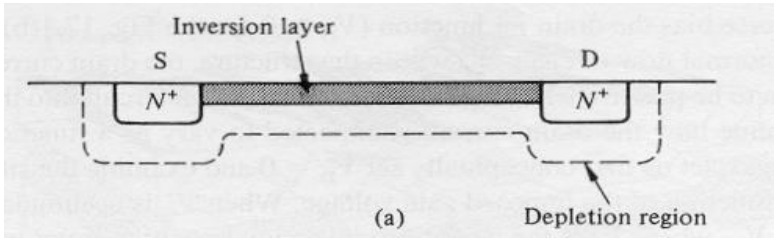
Sources: M. Lundstrom ECE 305 Slides

Recap: Theory of MOSFET (n-type)

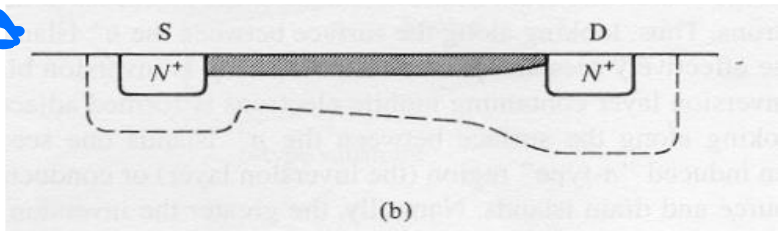
- When $V_{GS} < V_T$ the channel is depleted (off)
  $Q_{inv} = 0$



- When $V_{GS} > V_T$ the channel is inverted (on)
  $Q_{inv} \neq 0$



- If small drain voltage ($V_{DS} > 0$) is applied _____
  $I_D > 0$ if n-type; $I_D < 0$ if p-type



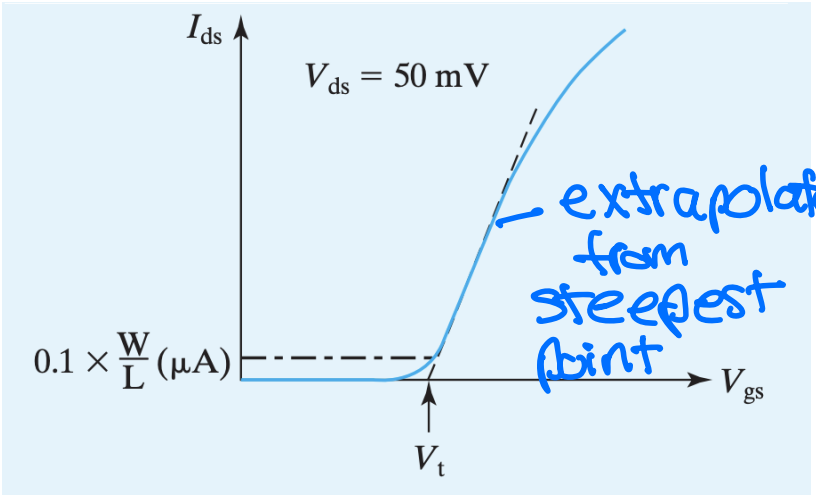
- Does sheet charge move by drift or diffusion?
  - Current ≈ width x sheet charge x velocity $= \frac{C}{s} = A$
- What is the inversion charge? $|Q_{inv}\ (\frac{C}{cm^2})|$ = $C_{ox}(V_{GS} - V_T)$ from MOS cap
- What is the drift velocity? v = $\mu E = \mu \frac{V_{ds}}{L}$
- Note: in reality, carrier mobility will be lower than bulk mobility due to surface scattering

Sources: E. Pop ECE 340 Slides

Metric: Threshold Voltage

- V_t (V): Threshold voltage, the minimum gate-to-source voltage (V_{GS}) that is needed to create a conducting path between the source and drain terminals and turn the device "on"
- Can be easily measured from the $I_D - V_{gs}$ transfer plot
- Extrapolate the steepest part of the measured V_{gs} curve back to $I_{DS}=0$
- Generally, lower V_t is preferable so high V_{gs} is not required for switching

Transfer Curve



NMOSFET

Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*

Current in the Linear Region (Low V_{ds})

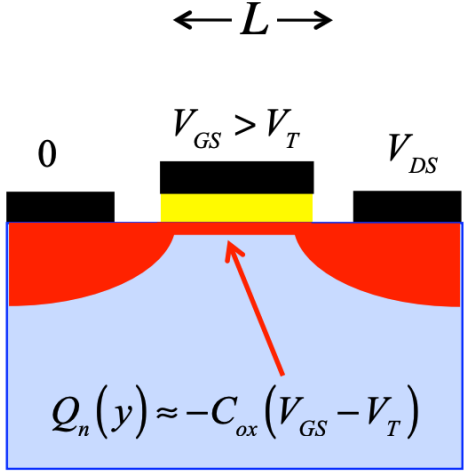
- At low V_{ds}, the inversion layer acts as a resistor

$$I_D = WQ_{inv}v = WQ_{inv}\mu_n E = WQ_{inv}\mu_n \frac{V_{DS}}{L}$$

$$I_D = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T) \cdot V_{DS} - \frac{1}{2} \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot V_{DS}^2$$

$$I_D = \frac{W}{L}\mu_n C_{ox} V_{DS}\left(V_{GS} - V_t - \frac{V_{DS}}{2}\right)$$

- First term represents drift, proportional to E-field
- Second term represents diffusion, which accounts for carrier gradients caused by the voltage drop V(x) along the channel

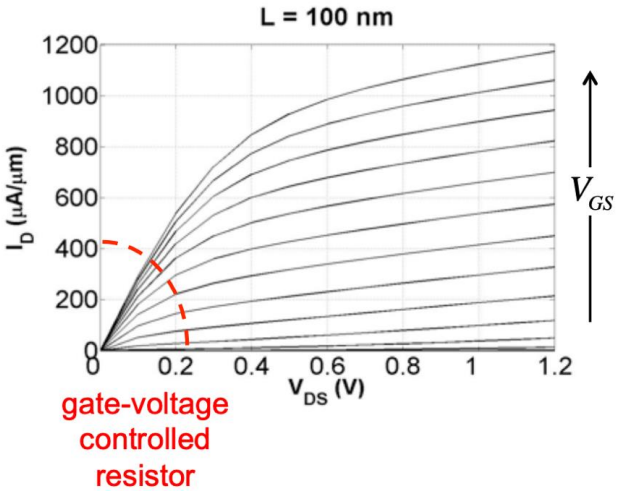


- W is the channel width (channel dimension perpendicular to the page), L is the channel length (parallel to page)
- Summary of relevant equations:

$$|Q_{inv}| = C_{ox}(V_{gs} - V_t)$$

$$|E| = \frac{V_{ds}}{L}$$

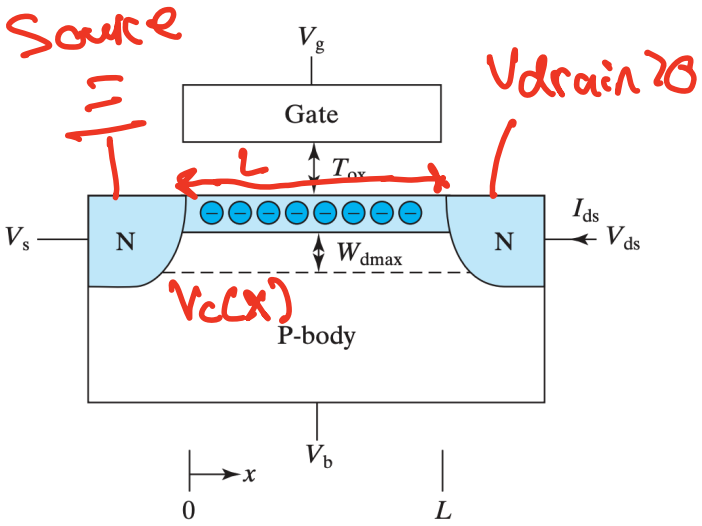
$$v = \mu E$$

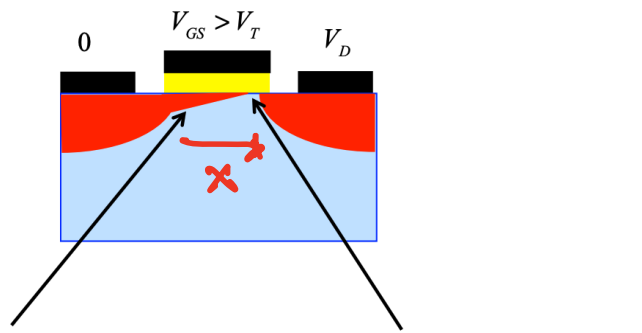


Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*, M. Lundstrom ECE 305 Slides

Channel Pinch-Off

- At higher V_{ds}, we must take into account variation in potential along the channel, $0 < V_c(x) < V_{ds}$
- Let $V_c = V_s$ at x = 0 and $V_c = V_d$ at x = L
- In the middle of the channel, $V_c\left(\frac{L}{2}\right) > V_s$ but $< V_d$
- Therefore, there total voltage across the capacitor will be less closer to the drain, so Q is less, and fewer e- in the inversion layer!
  - Recall: C = $\frac{Q}{V_{tot}}$
- $|Q_{inv}(x)| = C_{ox}(V_{gs} - V_t - V_c(x))$
- Eventually, the channel becomes completely pinched-off on the drain side at a point denoted
$$V_{d,sat} = V_{gs} - V_t$$
- The E-field is very high in the pinch-off region





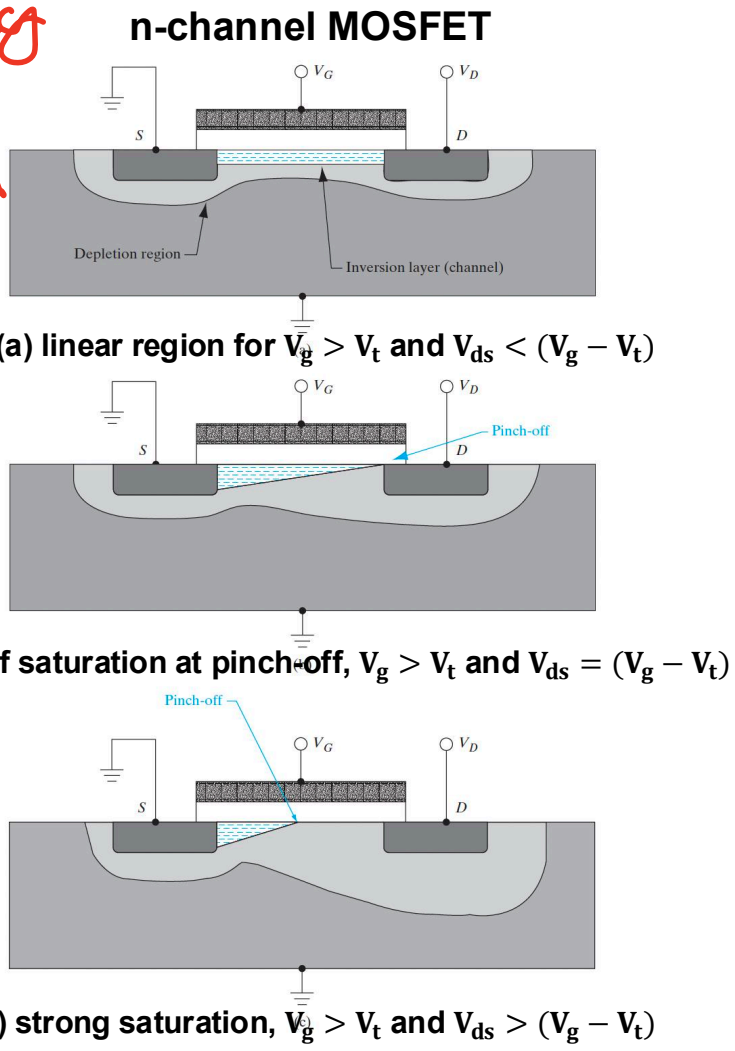
$$Q_n(y) = -C_{ox}(V_{GS} - V_T - V(y)) \qquad V(y_{pinch}) = (V_{GS} - V_T)$$

Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*, M. Lundstrom ECE 305 Slides

Channel Pinch-Off and Saturation

- What happens if we increase V_{ds} beyond $V_{ds,sat}$?
- The channel gets pinched off more and more!
- But how do carriers travel across the pinched-off region?
  - Due to high longitudinal E-field, e- in channel are pulled into pinch-off region
  - They travel at drift saturation velocity, v_{sat}
- So now, we have 2 competing effects. Any increase in V_{ds}
  - Reduces the amount of inversion charge, but…
  - Increases the lateral field (charge velocity)
- The two effects cancel out so that the current saturates to a value only dependent on V_{gs} (i.e. charge)
- I_d does not increase significantly with increasing V_{ds} beyond $V_{ds,sat}$
- But in reality I_d does increase a little. More on that in a minute.

& This is why Id is ≈ flat in saturation



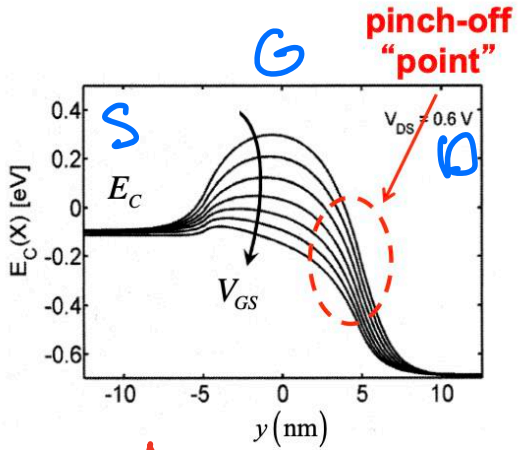
Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*

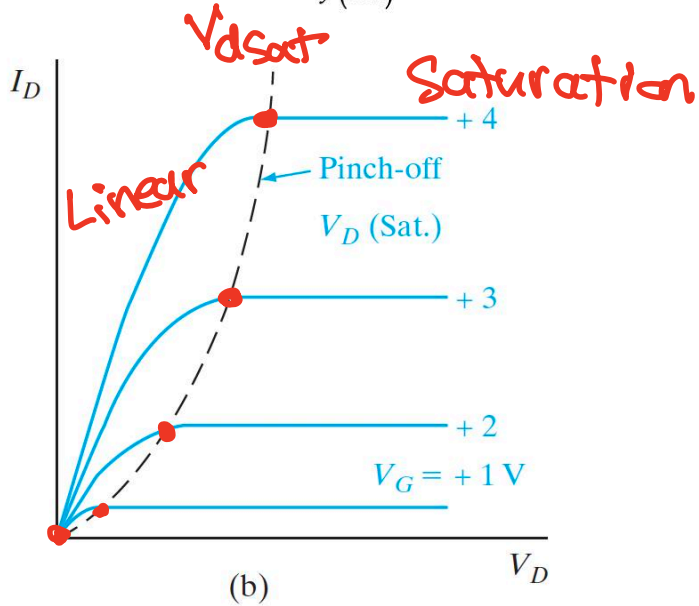
Metric: Pinch-off/Saturation Voltage

- So the recap, we've found that channel pinch-off occurs at the saturation or pinch-off voltage

$$V_{d,sat} = V_{gs} - V_t$$

- This point represents the transition from the linear to saturation region
- We can easily find $V_{d,sat}$ from the output characteristics
- For each Vgs, there is a different $V_{d,sat}$





Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*, M. Lundstrom ECE 305 Slides

Long Channel: Current in the Saturation Region (High V_{ds})

- Now that we know our variation of the inversion charge with channel distance x,

$$|Q_{inv}(x)| = C_{ox}\left(V_{gs} - V_t - V_c(x)\right)$$

- We can describe our current across a differential element dx at any point x as

$$I_d dx = \mu_n W |Q_{inv}(x)| dV_c$$

- If we integrate from source to drain, we get

$$\int_0^L I_d dx = \mu_n W C_{ox} \int_0^{V_{ds}} \left(\left(V_{gs} - V_t - V_c(x)\right) dV_c\right.$$

$$I_d = \frac{\mu_n W C_{ox}}{L}\left[\left(V_{gs} - V_t\right)V_{ds} - \frac{1}{2}V_{ds}^2\right]$$

- Since I_d is essentially constant in saturation, we can substitute in $V_{dsat} = V_{gs} - V_t$, and we finally get:

curve is flat

$$I_D = \frac{W}{2L}\mu_n C_{ox}\left(V_{GS} - V_T\right)^2 = \frac{W}{2L}\mu_n C_{ox} V_{d,sat}^2$$

Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*, M. Lundstrom ECE 305 Slides

Metric: Transconductance

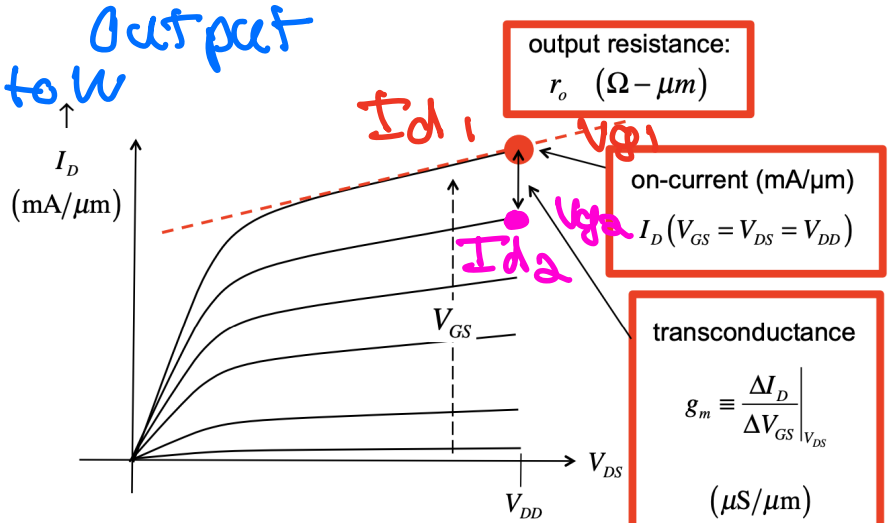
- g_m (S or $\frac{S}{\mu m}$*): Transconductance, change in drain current with change in gate-source voltage

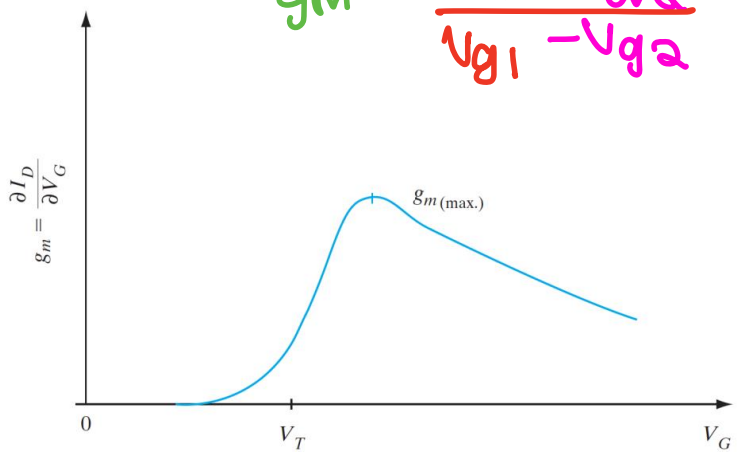
$$g_m \equiv dI_{ds}/dV_{gs}\big|_{V_{ds}}$$

- And can be easily obtained in the saturation region by differentiating our drain current eq. on previous slide w.r.t. gate voltage:

$$g_m(sat) = \frac{W}{L}\mu_n C_{ox}(V_{gs} - V_t)$$

- A measure of a transistor's sensitivity to the input voltage.
- In general, we want a large g_m (e.g. high sensitivity)
- We can plot $g_m - V_{gs}$
- The peak value is denoted $g_{m,max}$
- *Note: It is common to normalize the transconductance to channel width





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